# DESIGN OF A POWER PROTECTION SYSTEM COMPLIANT WITH MIL-STD-1275E

***Esim Akbulut*[1]*, *Ali Erduman*[2], *Gizem Hazar*[3]**

[1] Department of Electrical and Electronics Engineering, Sakarya University of Applied Sciences, Sakarya, Türkiye, esimakbulut@subu.edu.tr

[2] Hendek Vocational School, Sakarya University of Applied Sciences, Sakarya, Türkiye, alierduman@subu.edu.tr, 0000-0003-4116-3159

[3] Department of Electrical and Electronics Engineering, Sakarya University of Applied Sciences, Sakarya, Türkiye, gizemketenci@subu.edu.tr, 0000-0002-7142-8368

## Abstract

This study presents the design and simulation of an input power protection system for electronic subsystems used in military ground vehicles in compliance with the MIL-STD-1275E standard. MIL-STD-1275E defines stringent electrical limits to ensure the reliable operation of onboard electronics under harsh conditions such as voltage transients, load-dump surges, and reverse polarity events. Based on these requirements, practical electrical constraints are defined for the input protection stage and addressed through a surge-stopper-based circuit and PCB design. The proposed solution is implemented on a four-layer PCB with minimized current loop areas, separated power and signal paths, and distributed decoupling capacitors to enhance electromagnetic compatibility and thermal robustness. The effectiveness of the design is evaluated through time-domain circuit simulations performed in the LTspice environment under slow-rise (0–28 V), 100 V/50 ms surge, and reverse-polarity scenarios derived from the standard. During soft-start operation, the output voltage follows the input with a controlled delay of approximately 3.5–4.1 ms and reaches its nominal level within about 3 ms. Under surge conditions, the output voltage remains below 30.8 V, while reverse polarity operation safely disconnects the load by turning off the series MOSFETs. These results demonstrate that the proposed protection stage satisfies the electrical limits of MIL-STD-1275E and establishes a systematic, PCB level design methodology linking standard requirements, component level design equations, and circuit level validation. This approach enhances system reliability, protects sensitive electronic subsystems, and supports extended service life in military ground vehicle power systems.

**Keywords:** MIL-STD-1275E compliance, transient voltage protection, surge stopper (ltc4366-2), 28V military DC power systems, LTspice simulation and PCB design

## 1. INTRODUCTION

Reliability and durability in military systems are fundamental criteria for the system to operate successfully in the field. These systems are typically powered directly from sources such as engines, andincluding revisions to the Integrated Resource Plan (IRP), renewable energy procurement programmes, electricity pricing reforms, and targeted industrial restructuring. However, persistent dependence on coal-based generation, supply instability at Eskom, slow technological upgrading, and investment bottlenecks have limited the effectiveness of these batteries in harsh environments, such as military ground vehicles. This exposes electronic units to various electrical disturbances during engine operation, including voltage drops, sudden voltage surges (load dump) from generator connections, electromagnetic interference (EMI), and reverse polarity. Such adverse effects can lead to serious system failures, data loss, or functional malfunctions. Developed to prevent these effects, the MIL-STD-1275 standard specifies a set of electrical limits and protection criteria specifically for 28V DC power systems used in military vehicles. The most recent version of the standard specifies design requirements to ensure that equipment can operate safely both at its nominal operating voltage (25–30 VDC) and under abnormal conditions (e.g., a negative spike of -250 V or a positive transient of +100 V). Furthermore, considering the interference that must be suppressed in the 10 kHz to 50 MHz frequency range in terms of electromagnetic compatibility (EMC), it is evident that the standard aims to make the system resistant not only to electrical but also to environmental noise factors (U.S. Department of Defense, 2013). The control careful grounding, shielding and interconnection techniques, as widely discussed in electromagnetic compatibility literature.

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*Corresponding author: Esim Akbulut , esimakbulut@subu.edu.tr

Effective suppression of conducted and radiated noise in this band requires careful PCB layout, grounding strategy, and filtering techniques, as emphasized in fundamental EMC design principles (Morrison, 2016; Ott, 2009; Paul, 2006). Therefore, when designing a system compliant with the MIL-STD-1275 standard, it is necessary to consider not only a power protection circuit but also multilayered engineering principles such as signal integrity, thermal management, PCB layout, and filtering (Analog Devices, 2015; U.S. Department of Defense, 2013). In the literature, there are studies that examine various passive/active protection methods by modeling transient events in military vehicle power systems and analyzing conditions such as load drops and sudden voltage surges. Table 1 has been created to show the focus points of some of the studies conducted in this context.

As seen in Table 1, existing studies address protection approaches for transient events such as voltage surges, sudden rises, and load-dump conditions in 28 V DC military power systems and examine their compliance with the MIL-STD-1275E standard. These works provide valuable insights into transient modeling, protection concepts, and standard interpretation at the component or functional level. However, despite the availability of reference designs and review-oriented studies, there remains a clear need for implementation-focused examples that explicitly bridge the gap between formal standard requirements and practical hardware realization. In particular, existing studies rarely present a unified approach that connects the voltage–time envelope defined by MIL-STD-1275E with component-level design equations, PCB layout and electromagnetic compatibility considerations, and circuit-level time-domain validation. As a result, guidance on translating standard-defined transient limits into a reproducible, PCB-level input protection stage suitable for military vehicle applications remains limited. To address this need, the present study examines the technical requirements of MIL-STD-1275E in detail and presents an application-oriented input power protection design developed in accordance with these requirements.

The primary objective is to prevent damage to sensitive electronic loads caused by load transitions, voltage surges, and spike-like transient events encountered in military ground vehicle power systems. In this context, a front-end architecture incorporating complementary protection mechanisms is adopted, as given in Figure 1.

| Ref. | Technical Focus | Relevance to MIL-STD-1275E |
|---|---|---|
| (U.S. Department of Defense, 2013) | Standard defines voltage ranges, transient envelope, cranking, load dump, and reverse polarity limits for 28 VDC military ground vehicle power systems. | The standard defines the boundary conditions for transient events on 28 VDC lines and is therefore used as a basis for comparison for all technical designs. |
| (Aktas, 2019) | Control-based backup power and battery charging circuit that limits voltage fluctuations against load changes. | The study aims to comply with the voltage tolerances specified in MIL-STD-1275E by limiting sudden surges in 28 VDC power lines. |
| (Aktas, 2020) | Adaptive charging algorithm and hardware application that takes battery temperature into account | The charging circuit is designed to withstand voltage disturbances in accordance with MIL-STD-1275E and related military power standards. |
| (Pashaei, 2024) | Design of a 115 V AC power supply for aviation applications; overvoltage, overcurrent, and short-circuit protection. | In the design, compliance criteria with military standards such as MIL-STD-704F, MIL-STD-1275E, and similar standards are taken into account. |
| (Jordan, 2017) | Analysis of transient events such as surges/spikes in DC power systems in military vehicles and protection strategies against them. | MIL-STD-1275 transient test profiles are described in detail, defining 100 V/50 ms rollers and negative spike conditions. |
| (Texas Instruments, 2022) | Reference circuit compliant with MIL-STD-1275E, featuring a MOSFET-based active protection structure, operating within a 3–65 V input range. | The design provides hardware-based protection against MIL-STD-1275E test voltage waveforms (surge, spike, undervoltage). |
| (Ferguson, 2019) | Technical review explaining the requirements of MIL-STD-1275, its test methodologies, and its relationship with other military standards (such as MIL-STD-461). | Contains general explanations related to the standard. Does not contain design content, but explains the fundamentals of MIL-STD-1275E requirements. |
| (Doyle & Ochoa, 2023) | The study includes changes in the MIL-STD-1275F revision, particularly load dump (5 × 500 ms) and spike comparisons. | As the differences with revision F of the standard are explained, it can be used directly in the “future work” section; revision E provides technical support for the extension of designs. |

*Table 1 Selected Studies Related to Transient Protection and MIL-STD-1275E Compliance in 28 VDC Military Power Systems*

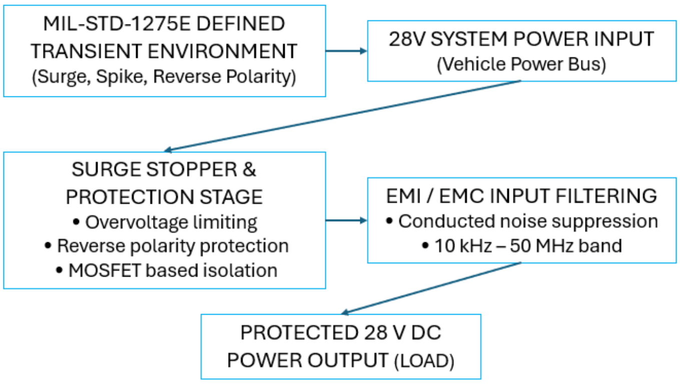

*Figure 1 : Overview of the proposed front-end protection architecture for MIL-STD-1275E-compliant 28 V DC power systems.*

The architecture shown in Figure 1 combines a surge-stopper-based overvoltage protection stage with MOSFET-based isolation and EMI/EMC input filtering to mitigate standard-defined transient disturbances before power is delivered to the load. This structured front-end approach enables a controlled response to overvoltage, reverse-polarity, and conducted-noise conditions specified by MIL-STD-1275E, while also supporting compact implementation and PCB-level robustness. Accordingly, this study examines whether a surge-stopper-based front-end protection architecture, derived directly from the voltage–time limits of MIL-STD-1275E, can maintain the load voltage within safe operating bounds under representative transient conditions. The proposed circuit structure therefore provides a reliable, scalable, and implementation-oriented power protection solution suitable for integration into military vehicle electronic subsystems. This paper is organized as follows. The Materials and Methods section describes the proposed system architecture in detail, including the selected hardware components, their characteristics, and the PCB design, with particular emphasis on EMI/EMC considerations. The Results section presents the simulation setup and the results obtained under representative transient scenarios derived from MIL-STD-1275E. The Discussion section addresses the implications and limitations of the proposed design in relation to existing work, and the Conclusions section summarizes the study and outlines directions for future research.

## 2. MATERIALS AND METHODS

### *2.1 Design Requirements from MIL-STD-1275E*

MIL-STD-1275E specifies the electrical characteristics of 28 V DC input power to utilization equipment in military vehicles, including nominal voltage ranges, cranking conditions, load-dump transients, spikes, and reverse-polarity events. For the purposes of this work, the following requirements are taken as design constraints for the input protection stage:

- Nominal operating range: the equipment shall operate without damage and within specified performance limits for input voltages between 25 V and 30 V DC.
- Slow-rise condition: the power bus may ramp from 0 V up to the nominal operating range; the protection stage shall ensure a controlled connection of the load without excessive inrush.
- Positive transient surge: the bus voltage may rise to 100 V and remain at this level for up to 50 ms, followed by a decay towards approximately 33 V within 500 ms. The protection circuit shall prevent the load from seeing damaging overvoltage during this event.
- Undervoltage conditions: during transient events, the input may drop to approximately 18 V for up to 500 ms, followed by recovery towards 20 V and nominal levels. The system shall avoid false operation under such sags.
- Reverse-polarity condition: accidental reversal of the supply leads shall not result in permanent damage; the protection stage shall block current to the load.

These requirements define the maximum allowable voltage and time envelope at the load side. In particular, the design target adopted in this work is to keep the load voltage below approximately 30.8 V under the +100 V surge condition, while maintaining normal operation in the nominal range and ensuring complete isolation during reverse-polarity events.

### *2.2 Component Selection and Design Equations*

The proposed architecture consists of a high-voltage surge-stopper integrated circuit (LTC4366-2) driving series N-channel MOSFETs, combined with input filtering, transient suppression devices, and a current-sensing shunt resistor. An overview of the main components and their functions is given in Table 2.

| Component | Model | Function |
|---|---|---|
| Overvoltage Protection IC | LTC4366 (Analog Devices, 2015) | Detects overvoltage conditions and controls series MOSFETs to protect the load |
| Low RDS(on) MOSFET | FDB44N25 (ON Semiconductor, 2013) | Provides high current capability with fast switching and low conduction loss |
| Surge Suppression Controller | LTC7860 (Linear Technology Corporation, 2015) | Controls large voltage changes and manages load-dump energy via a high-efficiency switching architecture |
| Reverse Current Diode (Schottky) | STPS30M100 (STMicroelectronics, 2018) | Protects the system against reverse current flow and supports reverse-polarity blocking |
| Zener / TVS Diodes | CMHZ5221B (Central Semiconductor, 2024) and TVS devices | Clamp fast voltage spikes above threshold and provide secondary surge protection |
| Input Filter | 33 µH Inductor, 150 µF Hybrid Capacitor | Forms an LC input filter to suppress high-frequency noise and improve EMI performance |
| Shunt Resistor | 4 mΩ | Enables input current monitoring and possible overcurrent detection |
| Ceramic Capacitors (X7R) | 1 µF, 0.47 µF, 10 µF | Provide local decoupling, stabilize the supply, and attenuate high-frequency noise at critical nodes |

The LTC4366-2 monitors the input voltage and controls the gate of the series MOSFETs to disconnect the load under overvoltage conditions. The overvoltage threshold, $V_{OV}$ , is set by a resistor divider connected to the FB pin. If we call the upper and lower resistors $R_{TOP}$ and $R_{BOT}$, and the internal FB reference voltage $V_{FB}$, the overvoltage threshold is calculated using equation 1:

$$V_{OV} \approx V_{FB}(1+R_{BOT}/R_{TOP})$$

This value is used to select the divider values so that the MOSFETs are turned off when the input exceeds the desired clamp level. In the presented design, the divider is chosen such that the output is limited below 30.8 V during the 100 V surge scenario.

The series MOSFETs are selected to withstand the maximum surge voltage and current with appropriate safety margins. Their drain-source voltage rating is chosen higher than the maximum possible surge amplitude, while their continuous current rating and RDS(on) are selected according to the expected load current and thermal limits.

A low-value shunt resistor of 4 mΩ is placed at the input to enable current monitoring and optional overcurrent detection. The corresponding voltage drop across the shunt is given by equation 2, which remains small under nominal load currents but can be used by supervisory circuits if extended protection schemes are implemented.

$$VSHUNT = Iin \times RSHUNT$$

To attenuate high-frequency components of the surge and improve EMC performance, an input LC filter is implemented using a 33 µH inductor and 150 µF hybrid capacitor. The corner frequency fc of the filter is calculated approximately as shown in equation 3:

$$fc \approx \frac{1}{2\pi\sqrt{LxC}}$$

This frequency is selected to effectively reduce high-frequency ringing and conducted noise without inducing excessive voltage overshoot or instability.

Additional Zener diodes and TVS structures are included to clamp very fast spikes and provide a secondary line of defense against voltage excursions beyond the MOSFET's safe operating area. Fast-response Schottky diodes such as STPS30M100 are used to prevent reverse currents and to support the reverse-polarity protection function. Distributed X7R ceramic capacitors (e.g., 1 µF, 0.47 µF, 10 µF) are placed close to critical pins to locally decouple the supply and to shape the transient response at high frequencies.

### *2.3 Electronic Card Design*

During the design process, comprehensive measures were taken to ensure EMI/EMC compliance and to provide protection against adverse conditions such as sudden voltage changes (transients) and reverse polarity that may occur at the power input. The PCB layout was designed with minimized loop area and separated power/signal paths, following well established EMC design principles such as controlled return paths and reduced parasitic inductance

(Morrison, 2016; Ott, 2009). Engineering techniques such as input filtering, transient suppression, and low impedance path design were applied to prevent transient events on the power lines from affecting system performance. On the PCB, high current lines and sensitive signal lines have been isolated from each other, and power and signal paths have been routed on separate layers. This has both reduced electromagnetic radiation and increased signal integrity. The power protection circuit design was implemented using the Altium Designer program (Altium LLC., 2025).

As shown in Figure 2, the developed protection circuit is designed to ensure system safety against sudden voltage changes and overvoltage events defined in the MIL-STD-1275E (U.S. Department of Defense, 2013) standard. The power input is supplied from a 28V DC source, and the system receives power through the MP1 and MP2 connectors. The P1 and P2 connection points are configured for input and grounding.

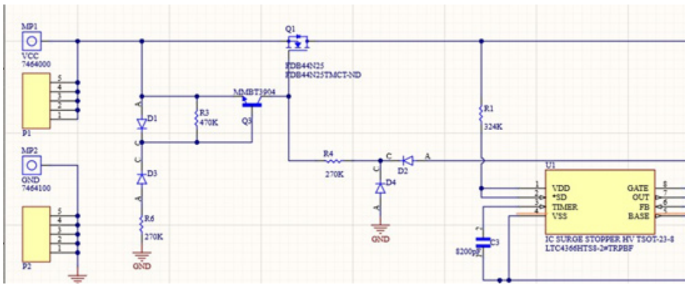

*Figure 2 : Load Protection Circuit Compliant with MIL-STD-1275E Standard*

The D1 and D3 diodes located on the input line form the first layer of protection against possible reverse polarity connections and sudden voltage spikes, for which TVS-based suppression components are widely recommended to ensure fast clamping during transient conditions. Thanks to this structure, reverse connections or high-frequency spikes that could damage the system are filtered out and prevented from reaching the load side. The MMBT3904 (onsemi, 2024) transistor (Q3) and resistors R3 and R6, working in conjunction with diodes D1 and D3, intervene at the gate of the MOSFET (ON Semiconductor, 2013) when the input voltage exceeds a certain threshold, preparing to isolate the load.

The main switching element of the system, Q1 (FDB44N25 MOSFET) (ON Semiconductor, 2013), is normally open under normal operating conditions and directly transmits the input voltage to the load side. However, in overvoltage conditions, it opens the circuit to protect the load. Diodes D2 and D4, used for the proper control of Q1, intervene quickly in the event of an overvoltage condition to support the driving of the MOSFET.

The main integrated circuit providing the system's protection management is the surge stopper integrated circuit with model number LTC4366HTS8-2#TRPBF (Analog Devices, 2015). This integrated circuit continuously monitors the input voltage and, if the limits set via the feedback (FB) line are exceeded, quickly turns off the MOSFET, isolating the load from the mains. The 8200 pF ceramic capacitor (C3) used at the integrated circuit input filters high-frequency interference that may occur at the system input, creating a stable operating environment. Thanks to this structure, the system is protected against adverse conditions such as 100V transient surges, sudden voltage drops (cranking), and reverse polarity, as required by the MIL-STD-1275E (U.S. Department of Defense, 2013) standard, ensuring a stable and safe operating environment on the load side.

Under the MIL-STD-1275E standard, specific voltage-time limits are defined to ensure devices withstand transient events that may occur in vehicle power systems. The voltage envelope shown in Figure 3 summarizes acceptable transient voltage profiles for 28V DC systems and the durations associated with these profiles.

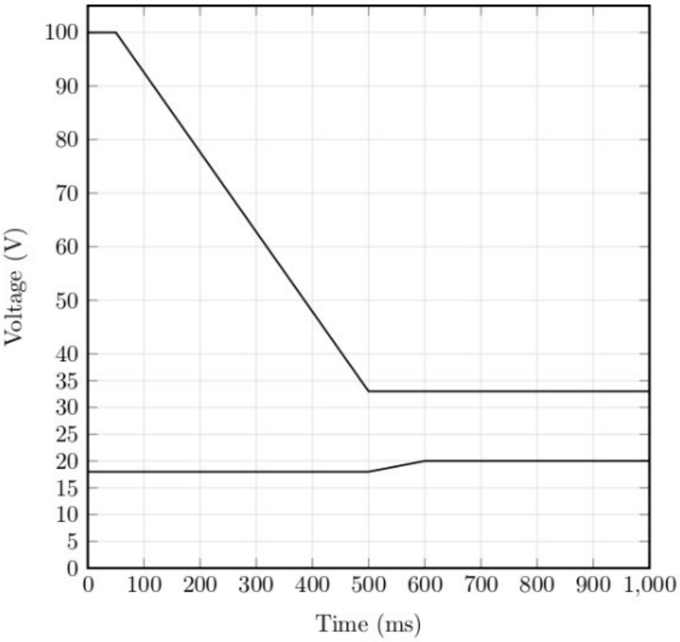

*Figure 3 : Transient voltage envelope defined for 28V DC systems according to MIL-STD-1275E (U.S. Department of Defense, 2013)*

At the beginning of the graph, the voltage instantly rises to 100V, and the duration of this high voltage is limited to 50 ms. Fast-clamping TVS devices are typically employed to limit such surge amplitudes before they reach sensitive. loads. At this level, devices are exposed to excessive voltage conditions for a short time, but permanent damage is prevented thanks to appropriate protective measures.

From this point onward, the voltage decreases in a controlled manner, falling to approximately 33V within 500 ms. 33V is close to the nominal operating voltage of the devices, and at this level, the devices can continue to operate safely.

The lower part of the graph defines low voltage conditions. During transient events, the voltage may drop to 18V for a short period, and this condition may persist for approximately 500 ms. If the voltage drops below 18V, the devices may become inoperable; therefore, this range has been defined as a critical threshold. The voltage then rises to 20V and remains stable at this level for 600 ms, allowing the system to recover.

The areas above and below the graphs in the Figure 3 indicate the voltage ranges where devices may be damaged or become inoperable. The area above the graph shows the range where devices are at risk of damage due to high voltage, while the area below the graph shows the range where devices lose functionality due to low voltage.

Based on this voltage-time profile, the MIL-STD-1275E (U.S. Department of Defense, 2013) standard requires power systems to be protected not only against overvoltage but also against undervoltage conditions. Therefore, it is crucial that the developed protection circuits are designed to provide both overvoltage suppression and undervoltage tolerance.

In the proposed protection stage, these amplitude and duration limits are used as target constraints when selecting the surge-stopper thresholds, MOSFET ratings, and LC filter values, and they also define the input waveforms applied in the LTspice simulations.

Figure 4 shows the three-dimensional PCB layout model of the power protection circuit designed in accordance with the requirements of the MIL-STD-1275E standard. The card design has been optimized to withstand high current and high frequency transient events.

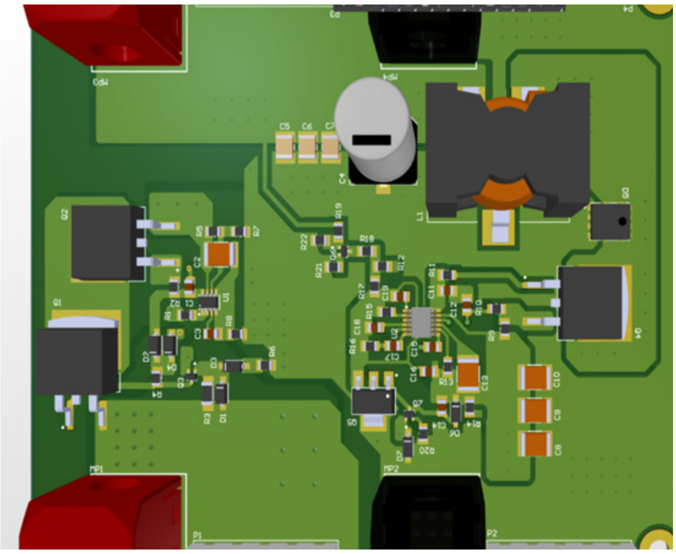

*Figure 4 : 3D View of MIL-STD-1275E Compliant Power Protection Card*

On the PCB, critical power components (MOSFETs, protection ICs, and high-current connectors) are positioned close to the input connector to minimize loop area, path resistance, and parasitic inductance during transient events, enabling the protection elements to respond quickly. The board uses a four-layer stack-up with continuous ground planes on the inner layers and 2 oz copper on high-current traces, providing low-impedance return paths and sufficient current-carrying capacity. Power and signal traces are routed on separate layers, and thermal vias are placed under MOSFETs and other hot-running components to improve heat spreading and temperature uniformity. This layout helps to reduce electromagnetic interference (EMI), improve signal integrity, and support a compliance-oriented design for the MIL-STD-1275E operating and transient conditions. The connectors on the card are selected to withstand the expected currents and the electrical and mechanical stresses associated with MIL-STD-1275E test profiles. The 3D view in Figure 4 reflects the actual physical structure of the protection card and illustrates how the layout has been optimized for electrical and thermal robustness. At this stage, however, the design has been validated only by LTspice simulations; no conducted or radiated emission measurements according to MIL-STD-461 and no hardware prototype, thermal measurements, or vehicle-level tests under MIL-STD-1275E conditions have yet been performed. Full MIL-STD-461 EMC testing and prototype validation in a representative vehicle power environment are therefore identified as important directions for future work.

## 3. RESULTS

The circuit shown in the Figure 5 demonstrates a power protection solution compliant with the MIL-STD-1275E standard, implemented using the LTC4366-2 integrated circuit. The circuit is powered by a 28V DC source and was tested in the simulation with a slowly rising input pulse from 0V to 28V. The Q1 and Q2 (IPB072N15N3)(Infenion, 2010) (equivalent) N-channel MOSFETs used in the circuit act as switching elements to protect the load. These MOSFETs are located on the output line controlled by the integrated circuit (U1). Soft switching is provided via the R2, C2, and D1 elements connected to the GATE pin to respond to rapid increases in the input voltage. The Q1 (2N3904) (ON Semiconductor, 2000) (equivalent) transistor connected in series to the input and the surrounding Zener diodes (D3, D4) provide additional protection to quickly turn off the MOSFET gate in case of excessive input voltage. Thus, the MOSFET gate is deactivated before the integrated circuit's own control time, improving the response time. Simulation results show that after a 0–28V ramptype surge applied to the input, the output voltage begins to rise with a delay of approximately 4.1 ms, then reaches 28V within 3 ms. This behavior indicates that the LTC4366-2's(Analog Devices, 2015) "surge stopper" function operates as expected and safely engages the load in the surge scenarios specified in MIL-STD-1275E. Additionally, the resistor divider (R7, R8) on the feedback (FB) line continuously reports the output voltage to the integrator, providing feedback to turn off the MOSFETs if the system exceeds its critical threshold. This structure prevents the output voltage from exceeding 30.8V, and it has been verified through simulation that the LTC4366-2 disconnects the load from the mains by cutting the MOSFET gates within its response time.

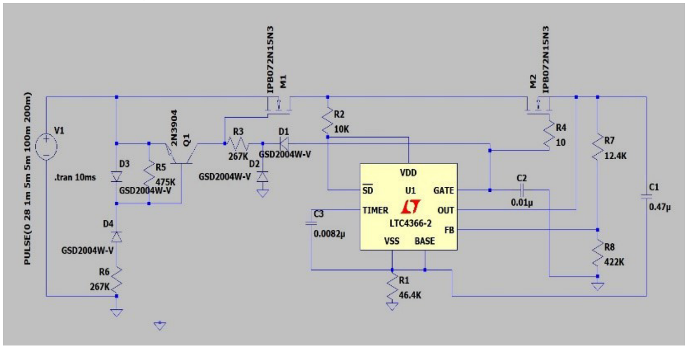

*Figure 5 : LTC4366-2 (Analog Devices, 2015)-Based MIL-STD-1275E(U.S. Department of Defense, 2013)-Compliant Power Protection Circuit (LTspice Schematic)*

Figure 6 shows the output voltage (VOUT) graph of the developed power protection circuit obtained in the simulation environment. The circuit is configured with the LTC4366-2(Analog Devices, 2015) integrated circuit and IPB072N15N3 (Infenion, 2010) (equivalent) N-channel MOSFETs (ON Semiconductor, 2013) and aims to examine the system's response to sudden surge input scenarios as specified in the MIL-STD-1275E (U.S. Department of Defense, 2013) standard. The input voltage is shown as the blue dashed line in the graph and was defined via the PULSE source to rise linearly from 0 V to 28 V starting at 1 ms. This was implemented to simulate the slow rise test scenario of MIL-STD-1275E. The output voltage, VOUT (orange line), did not start rising immediately after the input rise but began approximately 3.5 ms later.

This delay is the time required for the LTC4366-2 to analyze the input voltage, controllably raise the GATE pin, and ensure the MOSFETs transition to full conduction. The integrated circuit continuously monitors the output voltage and engages the load only if it does not exceed the specified FB reference voltage. Between 3.5 ms and 7 ms, VOUT shows a linear increase and reaches the 28V level in approximately 3 ms. This slope is shaped by the R7–R8 resistor divider, C1, and the MOSFET switching characteristics at the output. This gradual rise prevents sudden voltage spikes on the load, enhancing system stability. After 7 ms, the output voltage stabilizes and equals the input (VOUT ≈ VIN = 28V). At this stage, the system has entered normal operating mode and the LTC4366-2 is not in protection mode; the MOSFETs are conducting.

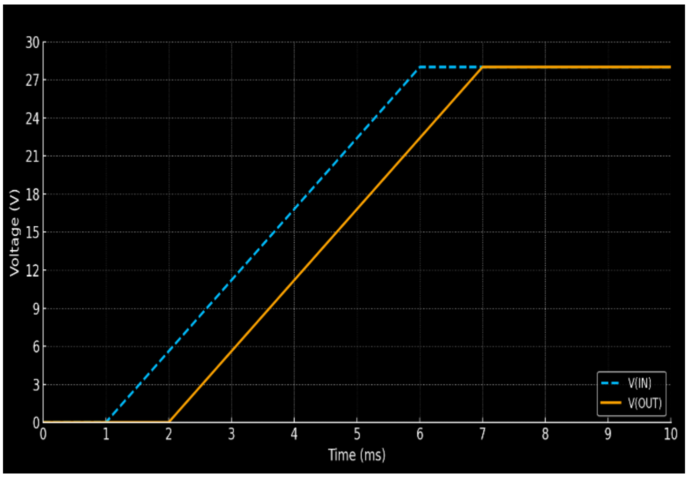

*Figure 6 : MIL-STD-1275E Compliant Circuit Output Voltage (VOUT) Behavior*

This graph in Figure 6 demonstrates that the system operates according to the principle of "providing a controlled and delayed output even if the input voltage rises rapidly."

| *Scenario* | *MIL-STD-1275E requirement* | *Simulated result* | |
|---|---|---|---|
| *Slow-rise input (0–28 V)* | *Output voltage shall remain within the nominal 25–30 V DC operating range without overshoot, even if the input rises rapidly* | *. After a 0–28 V ramp starting at 1 ms, VOUT begins to rise with a delay of about 4.1 ms and then reaches 28 V within approximately 3 ms, without overshoot above the nominal range.* | *Satisfied* |
| *100 V / 50 ms surge* | *For a 100 V surge lasting 50 ms, the equipment input shall not exceed the upper tolerance of the 28 V DC bus (≈33 V) and shall return to normal operation after the transient.* | *Under the 100 V / 50 ms surge profile, the output voltage VOUT is clamped and does not exceed approximately 30.8 V. After the surge, VOUT returns to the nominal operating range and normal conduction is restored* | *Satisfied* |
| *Reverse-polarity condition* | *During negative input transients, the load shall be protected against reverse voltage and the circuit shall prevent current flow into the equipment.* | *When the input is driven negative according to the reverse-polarity test profile, the MOSFETs remain off and the load node stays close to 0 V, so no reverse bias is applied to the load.* | *Satisfied* |

*Table 3: Summary of Simulation Results versus MIL-STD-1275E Limits*

This shows that it successfully meets the protection criteria specified in the MIL-STD-1275E standard and provides safe power transfer for critical military systems.To make this compliance more explicit, Table 3 summarizes the key simulated metrics for each test scenario and compares them with the corresponding MIL-STD-1275E limits.

As seen in Table 3, the proposed protection stage keeps the output voltage below the 33 V upper limit during the surge event, avoids overshoot during the slow-rise test, and effectively isolates the load under reverse-polarity conditions. These results quantitatively confirm that the simulated behavior of the circuit is consistent with the transient envelopes and operating limits defined in MIL-STD-1275E.

## 4. DISCUSSION

The simulation results presented in the previous section confirm that the proposed input protection stage can shape the MIL-STD-1275E transient profiles into safe conditions at the load side, but they also reveal the practical trade-offs of the chosen topology and component set. During the slow-rise test, the LTC4366-2 based architecture introduces a controlled delay and ramp at the output, which prevents sudden voltage application to downstream electronics. This behavior is particularly beneficial for sensitive digital modules and communication equipment, where inrush currents and fast overvoltage edges can otherwise lead to latch-up or premature component aging.

For the 100 V / 50 ms surge case, Table 3 shows that the output voltage remains below approximately 30.8 V, i.e., well under the ≈33 V upper tolerance of the 28 V DC bus defined in MIL-STD-1275E. This indicates that the selected MOSFET ratings, feedback divider, and LC filter values are sufficient to absorb the surge energy without overstressing the load. In addition, the reverse-polarity tests demonstrate that the MOSFET arrangement and diode network effectively block negative voltages, keeping the load node close to 0 V. Taken together, these findings suggest that the circuit can be used as a practical front-end protection stage or reference design for single-channel 28 V DC inputs in military ground vehicle applications.

The proposed design also needs to be viewed in the context of existing solutions summarized in Table 1. Many reference circuits and application notes focus either on high-level system considerations or on generic surge-stopper usage without providing a complete PCB-level implementation that explicitly targets the MIL-STD-1275E voltage–time envelope. In contrast, this work combines an LTC4366-2 based protection topology with a four-layer PCB layout, 2 oz copper on high-current traces, and an LC input filter sized according to the transient profiles. As a result, the contribution of the paper is primarily methodological and design-oriented rather than algorithmic: it shows how to translate the abstract transient limits of the standard into concrete component values, layout rules, and simulation scenarios that can be reused in similar platforms.

Despite these strengths, the study has several important limitations. First, all validation is based on LTspice simulations; no hardware prototype measurements are presented. Consequently, effects such as device tolerances, parasitic inductances and capacitances beyond those modeled, and temperature dependence have not yet been quantified. Second, while the PCB layout has been designed with EMI/EMC in mind (four-layer stack-up, ground planes, input filtering, and thermal vias), no conducted or radiated emission measurements according to MIL-STD-461 or environmental tests according to MIL-STD-810 have been performed at this stage. Therefore, the results should be interpreted as a proof-of-concept at circuit level rather than as a fully qualified subsystem.

Future work will address these limitations by implementing a hardware prototype of the protection card, performing transient tests with programmable power supplies that reproduce the MIL-STD-1275E surge, cranking, and spike profiles, and comparing the measured waveforms against the simulation predictions. In parallel, conducted and radiated emission measurements will be carried out according to MIL-STD-461, and environmental and durability tests will be considered in line with MIL-STD-810 procedures. Additional extensions may include adapting the topology to multi-channel inputs, integrating health-monitoring or diagnostic functions, and investigating alternative protection ICs or control strategies to optimize efficiency, cost, and board area.

## 5. CONCLUSIONS

In this study, a power protection stage compliant with the MIL-STD-1275E standard for 28 V DC military vehicle power systems was designed and evaluated. The proposed architecture combines an LTC4366-2 based surge-stopper topology with a four-layer PCB implementation, 2 oz copper on high-current traces, and an LC input filter sized according to the standard's voltage–time envelope. LTspice simulations under slow-rise, 100 V / 50 ms surge, and reverse-polarity conditions show that the circuit successfully limits the output voltage to approximately 30.8 V during the surge event, avoids overshoot during the 0–28 V ramp, and keeps the load node close to 0 V under negative input. These results confirm that the protection stage can maintain the load within the nominal operating window defined by MIL-STD-1275E while isolating it from severe transient disturbances.

Beyond verifying compliance at waveform level, the work demonstrates a practical design flow for engineers who must implement MIL-STD-1275E-compatible front ends in military ground vehicle electronics. By explicitly linking the transient profiles of the standard to component sizing, PCB layout rules, and simulation scenarios, the study provides a reusable reference for single-channel 28 V DC

inputs, bridging the gap between high-level standard requirements and detailed hardware realization.
The current work, however, is limited to circuit-level simulations and PCB-level design considerations. No hardware prototype measurements, no conducted or radiated emission tests according to MIL-STD-461, and no environmental or durability tests according to MIL-STD-810 have yet been performed. As future work, the protection card will be implemented as a hardware prototype and subjected to MIL-STD-1275E surge, cranking, and spike tests using programmable power supplies, with the measured waveforms compared against the LTspice predictions. In parallel, conducted and radiated emission measurements will be carried out in accordance with MIL-STD-461, and environmental tests following MIL-STD-810 procedures will be considered. Additional extensions may include adapting the topology to multi-channel power inputs and integrating monitoring or diagnostic functions to support condition-based maintenance in fielded systems.

**Conflict of interests**
The authors declare no conflict of interest

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